What is claimed is:

1. A stack package including two or more area array type chip scale packages, each chip scale package comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate;

a plurality of circuit patterns formed on the lower surface of the substrate and electrically connected to the ball land pads; and

one or more chips installed on an upper surface of the substrate and electrically connected to the circuit patterns,

wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner where the ball land pads of the upper stacked chip scale package face ~~in~~ the opposite direction as the ball land pads of the lower stacked chip scale packages, and wherein the circuit patterns of the upper stacked chip scale package are electrically connected to those of the lower stacked chip scale package.

2. The stack package according to claim1, wherein the circuit patterns of the upper stacked chip scale package are electrically connected to the circuit patterns of the lower stacked chip scale package by connecting boards.

3. The stack package according to claim 2, wherein each connecting board comprises a flexible film and wiring patterns formed on the film.

4. The stack package according to claim 1, wherein a hole is formed in the substrate of each chip scale package, and the chip is electrically connected to the circuit patterns by bonding wires passing through the hole.

5. The stack package according to claim 4, wherein a plurality of bonding pads of each chip scale package are formed on the central region of the chip and exposed through the hole, and wherein one end of each bonding wire is attached to a corresponding bonding pad of the chip.

6. The stack package according to claim 5, wherein the chip is protected by a first encapsulating part, and the bonding pads and the bonding wires are protected by a second encapsulating part.

7. The stack package according to claim 6, wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other by an adhesive applied on the first encapsulating part.

8. The stack package according to claim 1, wherein a plurality of solder balls is formed on the ball land pads of the lowest stacked chip scale package.

9. The stack package according to claim 1, wherein a single chip scale package is stacked on, and electrically connected through a plurality of solder balls to adjacently stacked chip scale packages coupled by connecting boards.

10. The stack package according to claim 1, wherein an adjacently stacked chip scale packages coupled by connecting boards are stacked on, and electrically connected through a plurality of solder balls to another adjacently stacked chip scale packages coupled by connecting boards.

11. The stack package according to claim 1, wherein a plurality of connection pads are formed on the outside of the region of the substrate on which a plurality of ball land pads are formed, and electrically connected to the circuit patterns.

12. The stack package according to claim 11, wherein connecting boards are electrically connected to the circuit patterns through the connection pads.

13. The stack package according to claim 12, wherein both ends of the connecting board at which the connecting board is attached to the connection pads are bent.

14. A method of forming a stack package of two or more area array type chip scale packages, the method comprising:

forming a lower chip scale package of an adjacent pair of chip scale packages including a substrate, a plurality of ball land pads and circuit patterns formed on a lower surface of the substrate, and one or more chips formed on an upper surface of the substrate;

forming an upper chip scale package of the adjacent pair of chip scale packages in the same manner as the lower chip scale package;

attaching the upper chip scale package to the lower chip scale package so that the ball land pads of the upper chip scale package face the opposite direction as the ball land pads of the lower chip scale package; and

electrically connecting the circuit patterns of the upper chip scale package to the circuit patterns of the lower chip scale package.

15. The method of claim 14, wherein electrically connecting the circuit patterns of the two chip scale packages of an adjacent pair of chip scale packages further comprises attaching flexible connecting boards to connection pads formed on the same surface of each chip scale package substrate as the ball landing pads.

16. The method according to claim 16, further comprising bending the ends of the connecting boards to attach to a larger surface of the connection pads.

17. The method of claim 14, further comprising:

forming a hole in the substrate of each chip scale package; and

electrically connecting the chip to the circuit patterns by bonding wires through the hole.

18. The method of claim 14, further comprising:

forming a first encapsulating part over an upper surface of each chip scale package and chip; and

forming a second encapsulating part over the bonding pads and bonding wires of each chip scale package.

19. The method of claim 18, further comprising attaching the two chip scale packages with an adhesive applied on the first encapsulating part of each chip scale package.

20. The method of claim 14, further comprising forming a plurality of solder balls on the ball lands of the lower chip scale package of an adjacent pair of chip scale packages.

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